AMENDMENT

To: Examiner of the Patent Office

1. Identification of the International Application

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4 . Item to be amended

Claims and Drawings

5. Subject Matter of Amendment

(1) Page 29, line 4, the word " non-volatile" should be inserted after "a" (first occurrence).

(2) Page 29, line 6, the expression "and a redundancy portion" should be inserted after "logical pages".

(3) Page 29, line 21, the word "second" should be inserted after "a".

(4) Page 29, line 21, the expression "for storing " should be amended as "which is randomly accessable and stores".

(5) Page 29, line 24, the word "third" should be inserted after "a" (first occurrence).

(6) Page 29, line 24, the expression "for storing " should be amended as "which is randomly accessable and stores".

(7) Page 29, line 26, the expression "when this memory device is activated, said controller reads the redundancy portions of said non-volatile memory and prepare the address translation table in said second memory and the write pointer in said third memory; " should be inserted after "empty logical page,".

(8) Page 31, line 3, the word " non-volatile" should be inserted after "managing a" .

(9) Page 31, line 5, the expression "and a redundancy portion" should be inserted after "one or more logical pages"

(10) Page 31, lines 19 and 20, the expression " in that it is discriminated" should be amended as "by further comprising the steps of: discriminating".

(11) Page 31, line 21, the word " that" should be amended as "specifying".

(12) Page 31, line 22, the expression " are specified and" should be amended as ", transferring".

(13) Page 31, line 23, the expression " is transferred" should be deleted.

(14) Page 31, line 24, the word " erasing" should be inserted after "and" .

(15) Page 31, line 24, the expression " is erased" should be deleted.

(16) Page 31, line 25, the word "non-volatile" should be inserted after "to a" .

(17) Page 31, line 27, the expression "and a redundancy portion" should be inserted after "one or more logical pages".

(18) FIG.6, the expression "BPT/BST" in box S101 should be amended as "BPT/BSI".

6. List of Attached Documents

(1) Replacement sheets of pages 29/1, 29/2, 31/1, and 31/2 of the claims.

(2) Replacement sheet of page 6 of drawings.

CLAIMS

1. (Amended) A memory device characterized by comprising:

a non-volatile memory (11) including a plurality of memory blocks which stores data and each of which is comprised of one or more physical pages each including one or more logical pages and a redundancy portion; and

a controller (12, S314, S308 to S310) which, when to-be-written data is supplied to said memory device, writes said to-be-written data in that empty logical page in said logical pages which is in a data storable state, discriminates whether to-be-replaced data to be replaced with said to-be-written data is stored in said logical pages, and writes validity data indicating that said to-be-replaced data is not valid in that physical page which includes said logical page that stores said to-be-replaced data, when having discriminated that said to-be-replaced data is stored in said logical page.

2. The memory device according to claim 1, characterized in that when information for specifying a to-be-read logical page to be read out is supplied to said memory device, said controller (12) specifies said to-be-read logical page based on said information, reads data from said specified to-be-read logical page and sends said read data outside (S201 to S214).

3. (Amended) The memory device according to claim 1, characterized in that physical addresses are allocated to said logical pages,

said memory device further comprises a second memory (123) which is randomly accessable and stores an address translation table representing a correlation between said physical addresses of said logical pages and logical addresses to be used to specify said logical pages by an external unit, and a third memory (123) which is randomly accessable and stores a write pointer that points the empty logical page in said logical pages which is in a data storable state and instructs the physical address of said specified empty logical

page,

when this memory device is activated, said controller reads the redundancy portions of said non-volatile memory and prepare the address translation table in said second memory and the write pointer in said third memory;

and

when to-be-written data and a logical address are supplied to said memory device,

information, reads data from said specified to-be-read logical page and sends said read data outside (S201 to S214).

9. (Amended) A memory managing method of managing a non-volatile memory (11) including a plurality of memory blocks which stores data and each of which is comprised of one or more physical pages each including one or more logical pages and a redundancy portion, characterized by comprising the steps of:

writing, when to-be-written data is supplied to said memory, said to-be-written data in that empty logical page in said logical pages which is in a data storable state (S314); and

discriminating whether to-be-replaced data to be replaced with said to-be-written data is stored in said logical pages, and writing validity data indicating that said to-be-replaced data is not valid in that physical page which includes said logical page that stores said to-be-replaced data, when it is discriminated that said to-be-replaced data is stored in said logical page (S308 to S310).

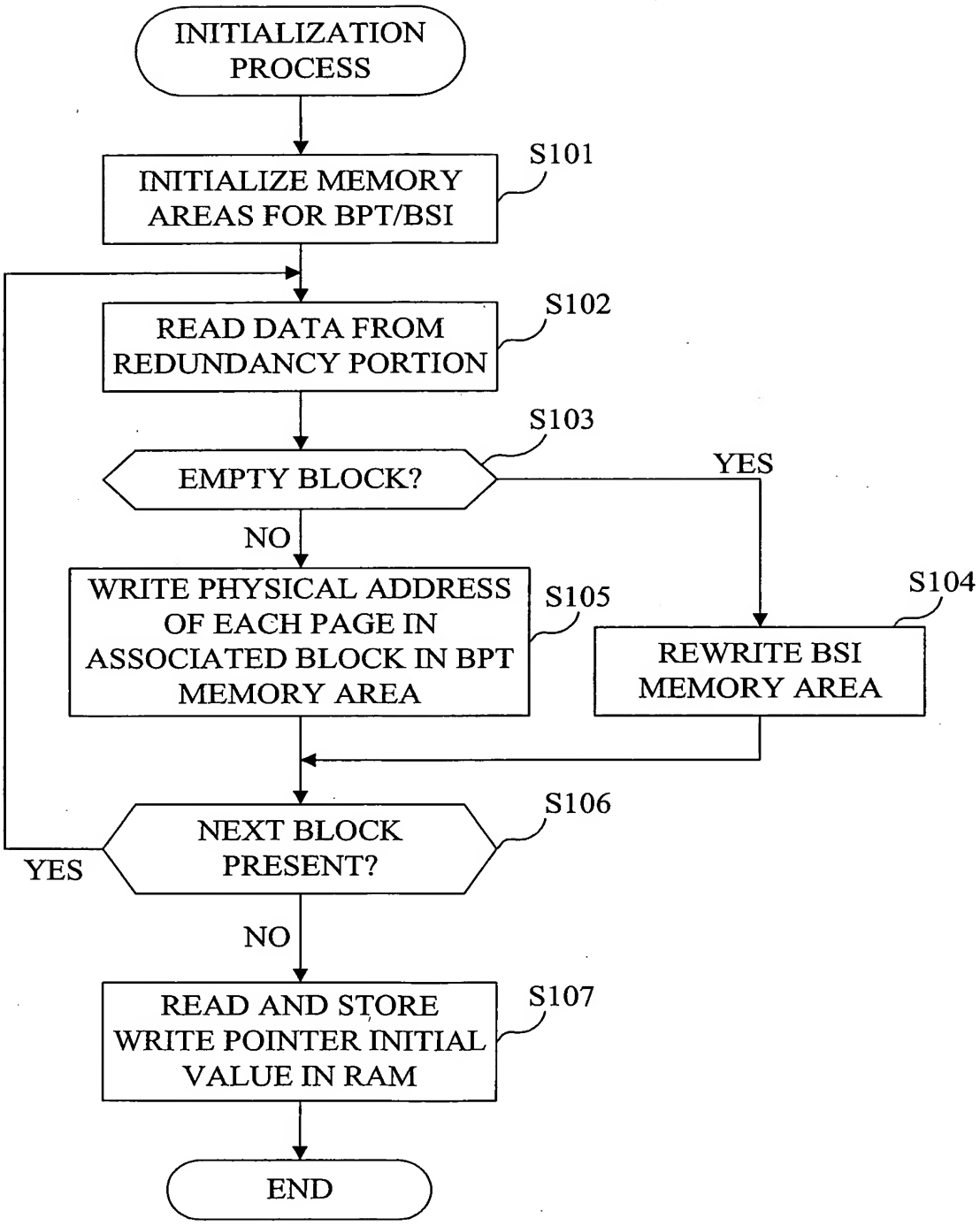
10. The memory managing method according to claim 9, characterized in that validity data indicating that said written to-be-written data is valid is written in that physical page which includes the logical page where said to-be-written data is stored (S314), that logical page where data is not stored is specified based on said validity data and said specified logical page is treated as said empty logical page.

11. (Amended)The memory managing method according to claim 10, characterized by further comprising the steps of: discriminating whether or not data stored in each of said logical pages in to-be-erased memory blocks is valid based on said validity data (S501), specifying a logical pages which are located in another memory blocks and where data is not stored, transferring the data which has been discriminated as valid into said specified logical pages (S502 and S503, S507), and erasing data stored in said to-be-erased memory blocks (S504).

12. (Amended)A program for allowing a computer (121), connected to a non-volatile memory (11) including a plurality of memory blocks which stores data and each of

which is comprised of one or more physical pages each including one or more logical pages and a redundancy portion, to function to:

FIG. 6


INITIALIZATION PROCESS
INITIALIZE MEMORY AREAS FOR BPT/BSI
S101
READ DATA FROM REDUNDANCY PORTION
S102
EMPTY BLOCK?
S103
YES
NO
WRITE PHYSICAL ADDRESS OF EACH PAGE IN ASSOCIATED BLOCK IN BPT MEMORY AREA
S105
REWRITE BSI MEMORY AREA
S104
NEXT BLOCK PRESENT?
S106
YES
NO
READ AND STORE WRITE POINTER INITIAL VALUE IN RAM
S107
END